Quiz 1 - COL 380 / COL 730 / COL7880 | Feb 13 2026

1. Consider the loop:

```
a[0] = 0;
for (i = 1; i < n; i++)
    a[i] = a[i-1] + i;
```

   Is the loop parallelizable (with or without loop transformation)? If yes, then write snippet of OpenMP code for the parallel version of this loop. If no, then explain why not. (10 Marks)

2. For each of the histories shown in the figure below, are they Sequentially consistent? Linearizable? Justify your answer. (8 marks)

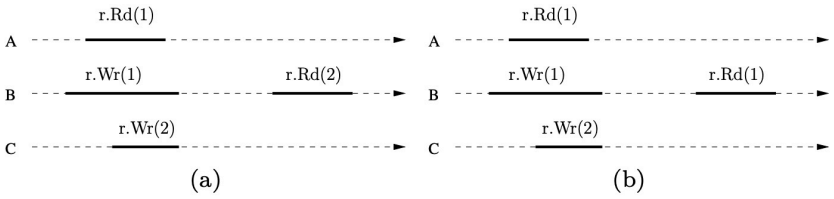

Figure 1: Figures

3. Consider four processors (P1 through P4) operating on two variables, X and Y, both initially 0. The system implements Processor Consistency and uses a snoopy-based MSI coherence protocol.

```
P1: X = 1

P2: Y = 1

P3: r1 = X; r2 = Y

P4: r3 = Y; r4 = X
```

   Is the outcome $r1 = 1, r2 = 0, r3 = 1, r4 = 0$ possible under Processor Consistency (explain your answer)? How does this differ from Causal Consistency? (6 Marks)

Check all that applies. Also explain your choices.

4. Which of the following statements regarding atomicity in concurrent systems are correct? (3 Marks)

   a. An atomic operation is one that appears to happen instantaneously from the perspective of other threads.

b. Atomicity violations can occur even if all individual memory accesses are themselves atomic.

c. Visibility through coherence ensures that compound operations (like count++) are atomic.

d. All of the above

5. Which of the following are properties or requirements of a correct solution to the Mutual Exclusion problem? (3 Marks)

   a. There is a limit on the number of times other threads can enter their critical sections after a thread has requested entry.

   b. If no thread is in its critical section and some thread wish to enter, only those not in their remainder section can participate in the decision.

   c. If one thread fails inside the critical section, other threads must be able to proceed into the critical section.

   d. Threads must take turns in a specific, fixed order.