Introduction to Parallel & Distributed Programming

Lec 01 — Course Logistics, Introduction

Subodh Sharma (a.k.a SVS) | Jan 02, 2026

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- 4 Lab Assignments, 2 In-class Quizzes, 1 Lab Exam, Minor, Major; Additional task — **Transcribing!**

Transcribing — Begins from the Next Class!

- Drafting of the entire lecture content **in Latex**
  - **Key learning outcomes** for that content
  - Key takeaways (5-10 bullet items)
  - In **2 to 3 examples to motivate** the topical discussion
  - Comprehensive references
  - **4-8 problems** and their solutions

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    - Synchronisations, Logical clocks, Consensus,

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- It’s a 2-0-2 course, but felt like 2-0-6 — **deal with it** and learn to start early!

Parallel, Distributed, Concurrency

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- **Parallelism:** Concurrency but **in close coordination**
  - **Eg: Matrix multiplication: Threads may share the same shared memory arrays**
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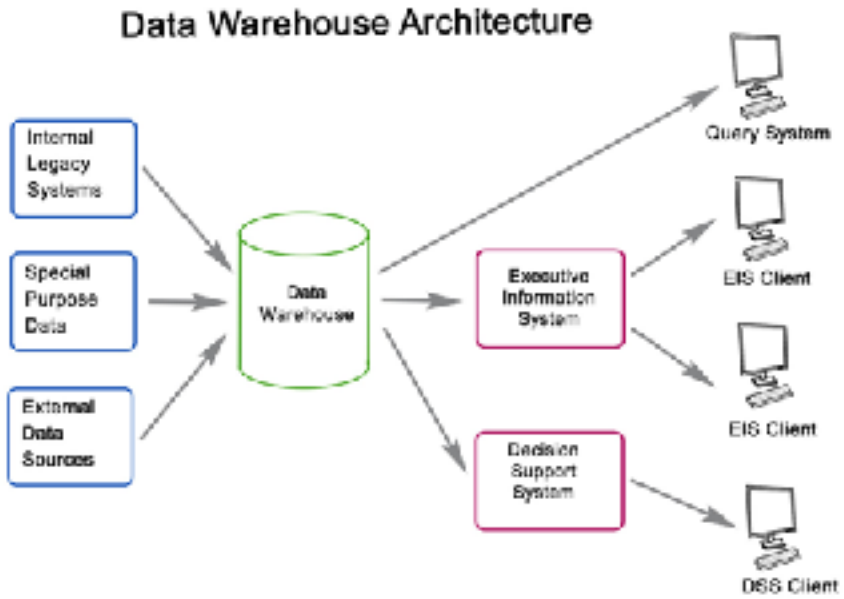

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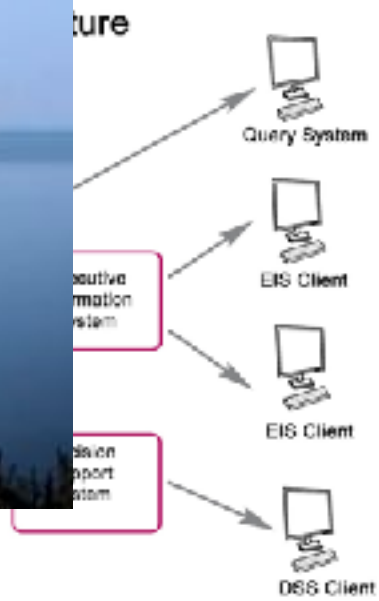

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Courtesy: Nano Banana

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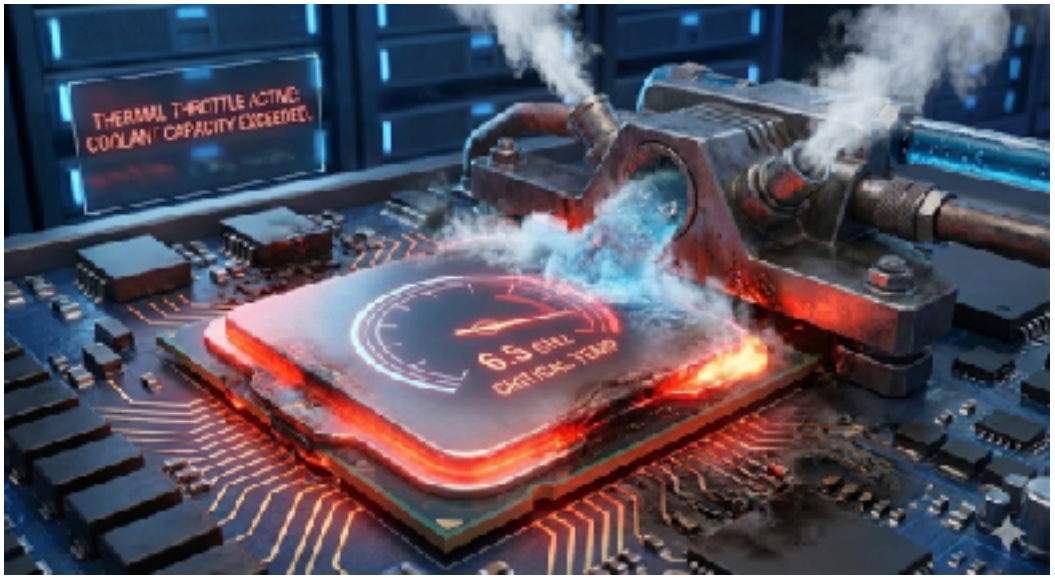

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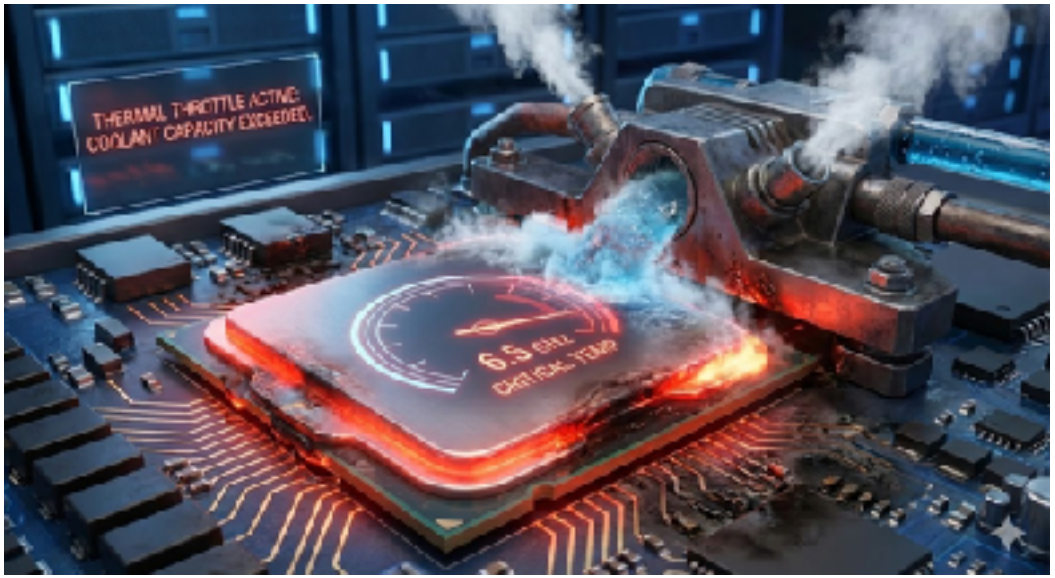
- **The V/F curve**: For $f \geq 5Ghz$, the physics break down, even to **get a jump of 100 MHz**, large jump in voltage is required



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Concurrency in Hardware

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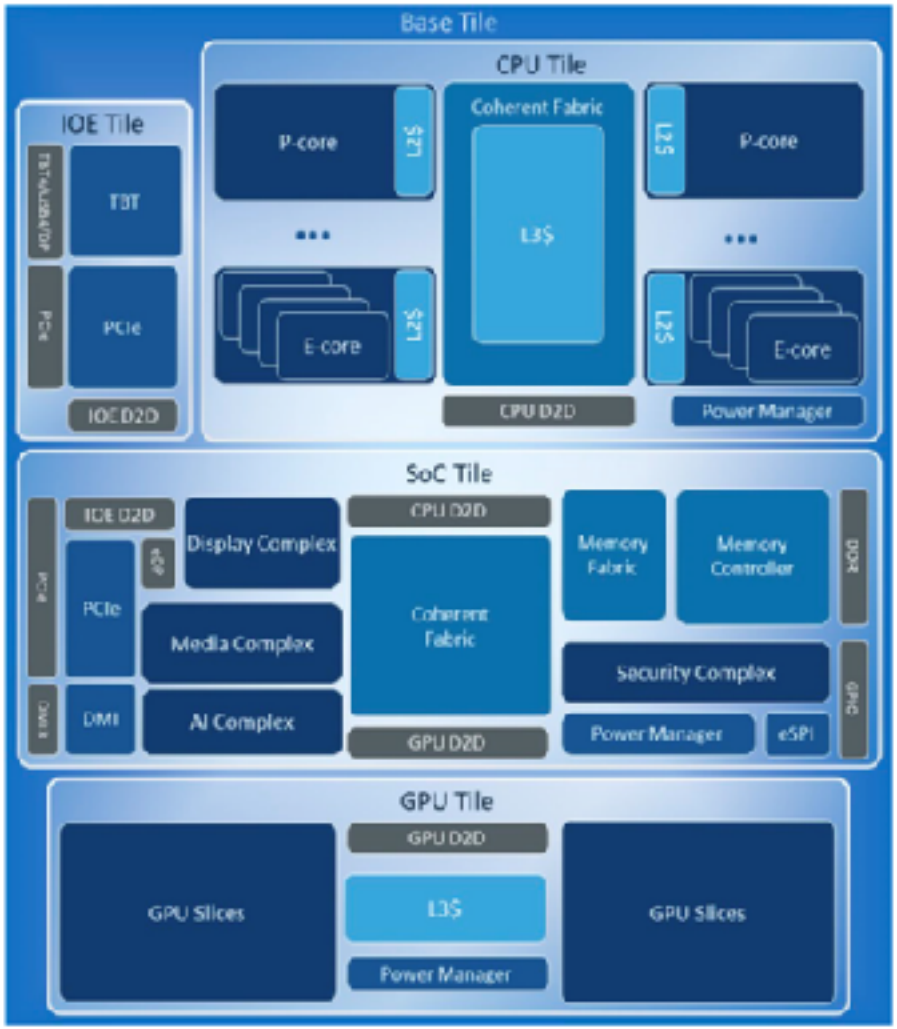

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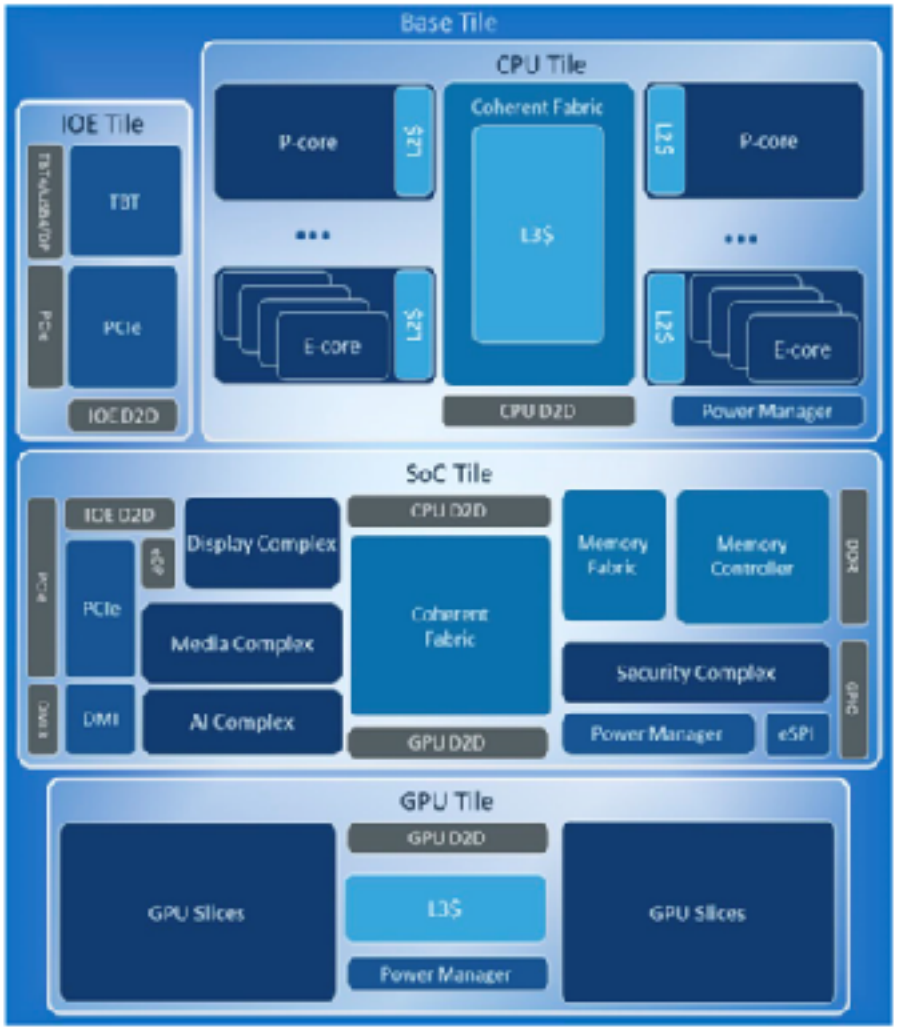

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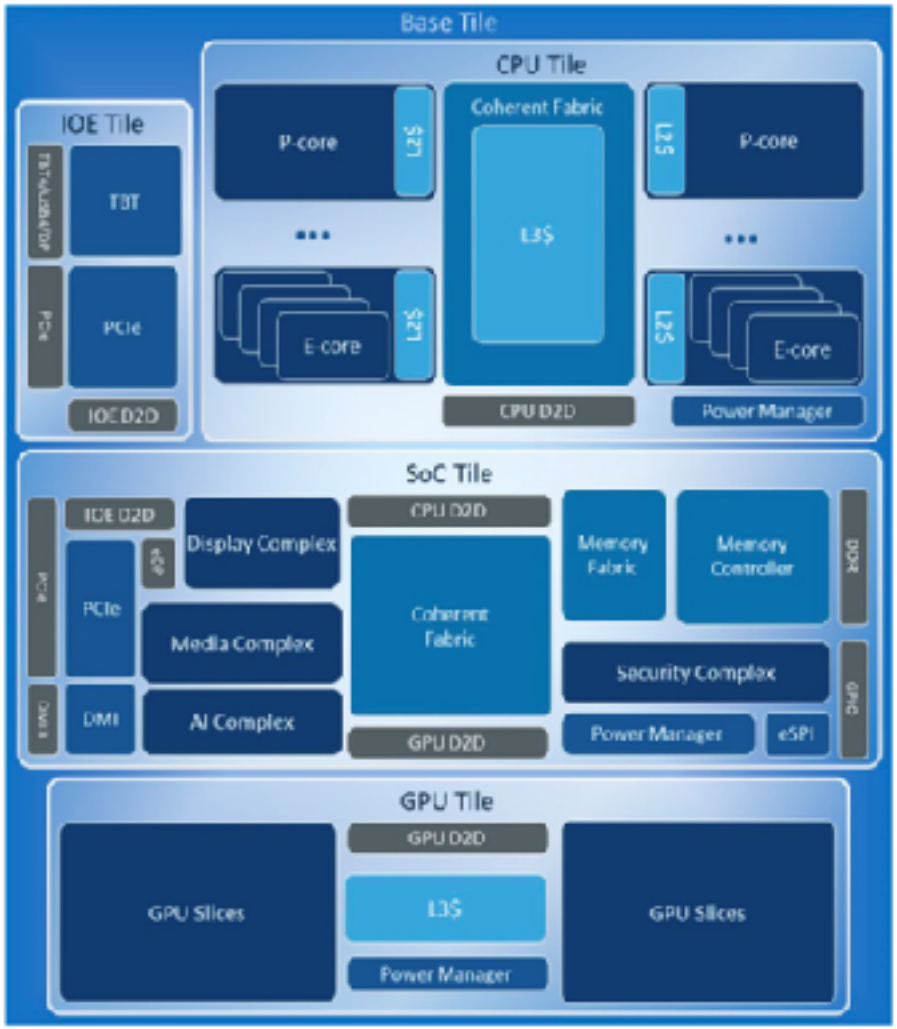

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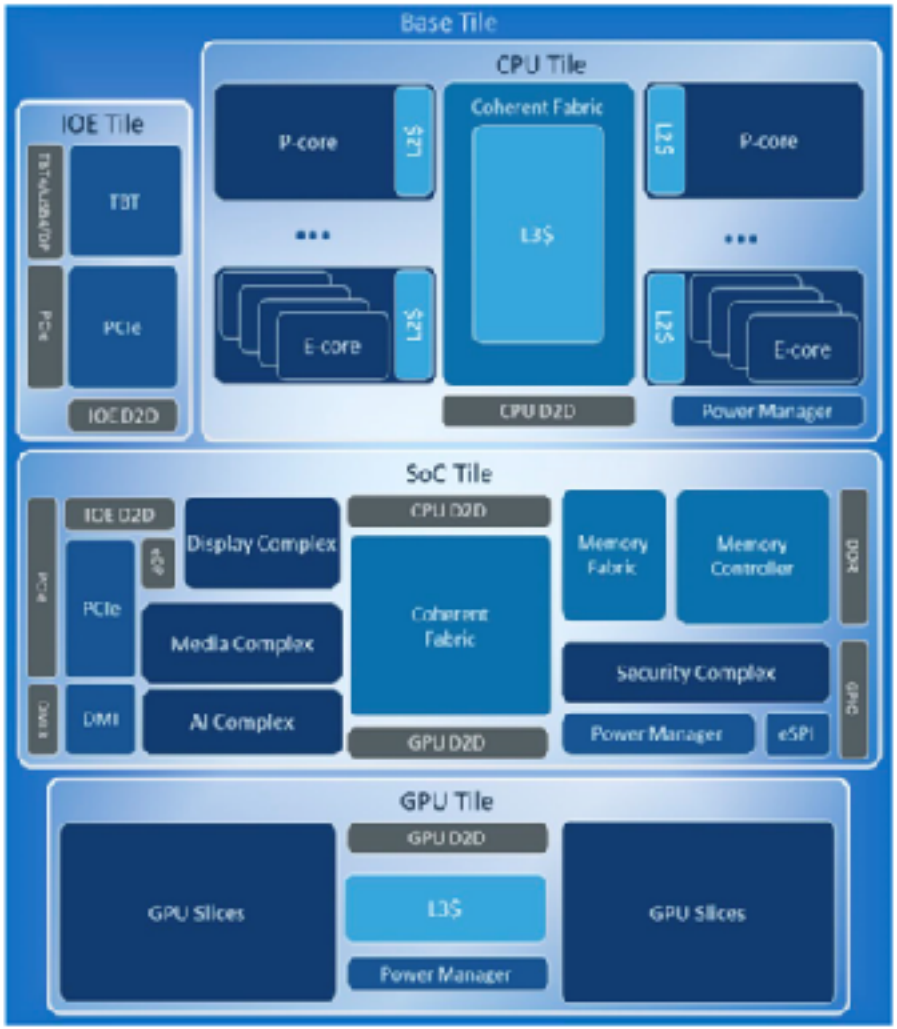

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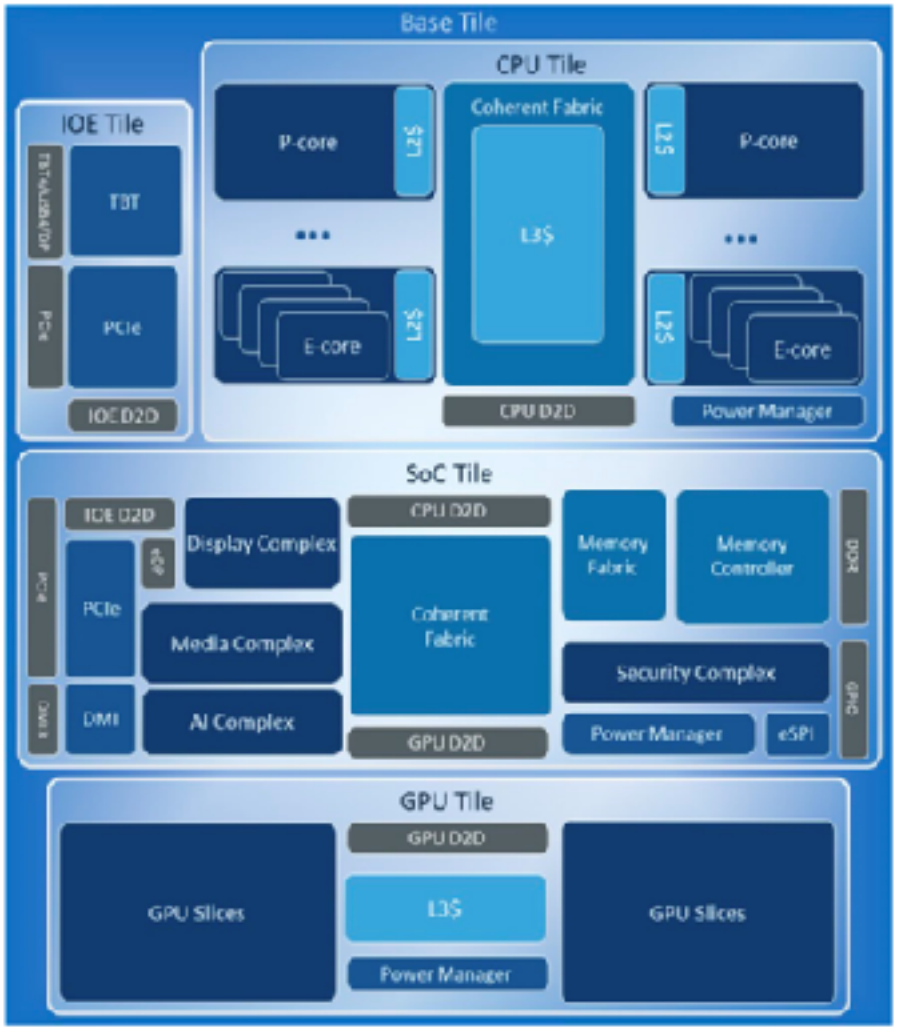

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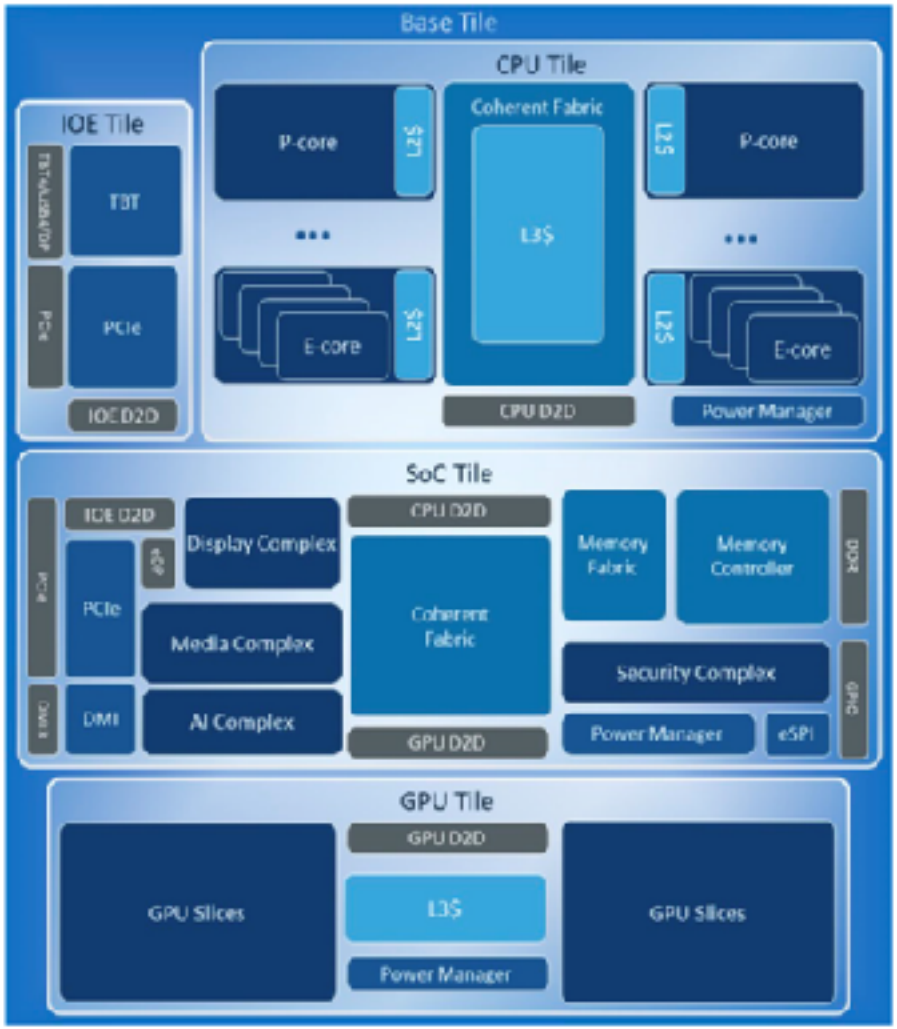

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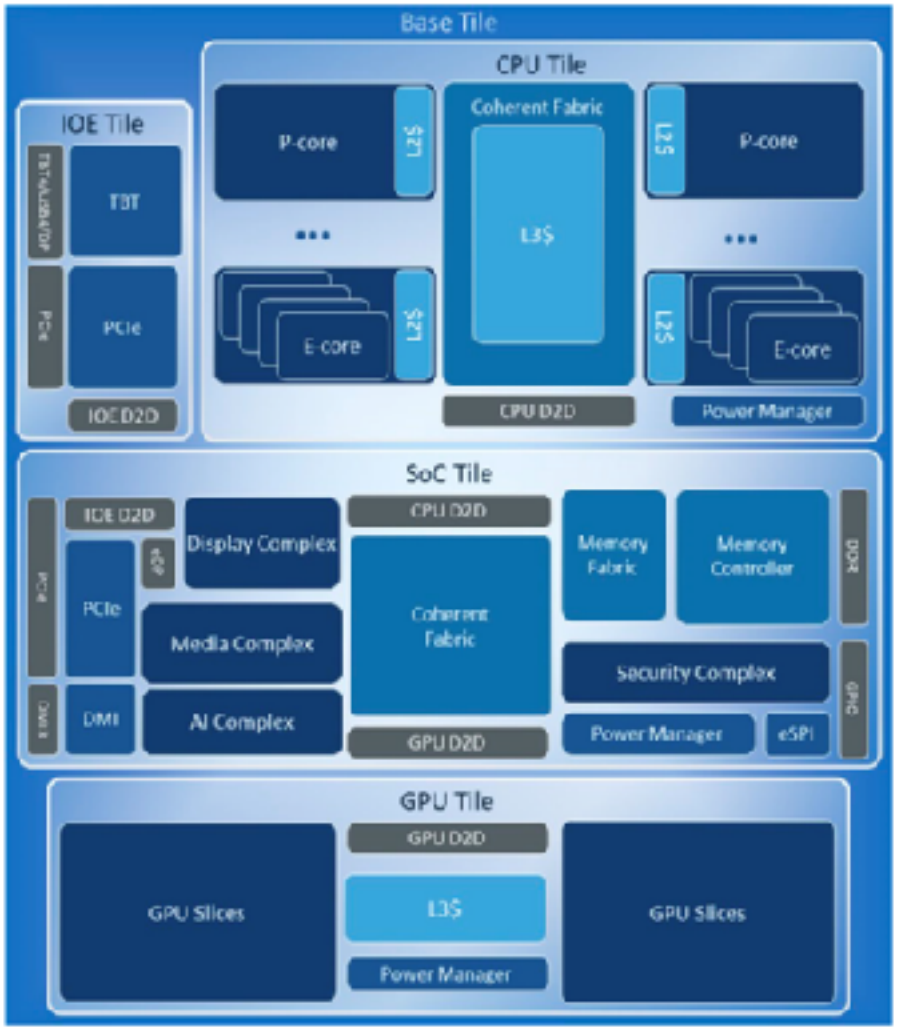

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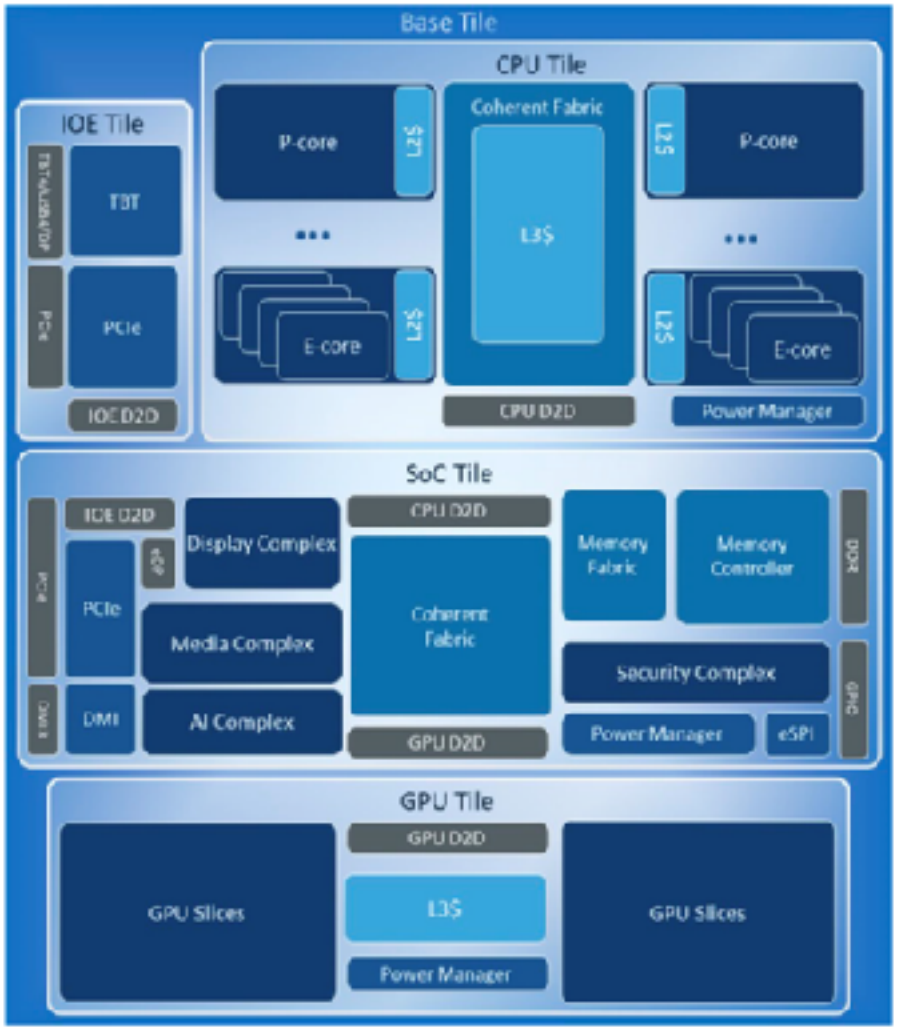
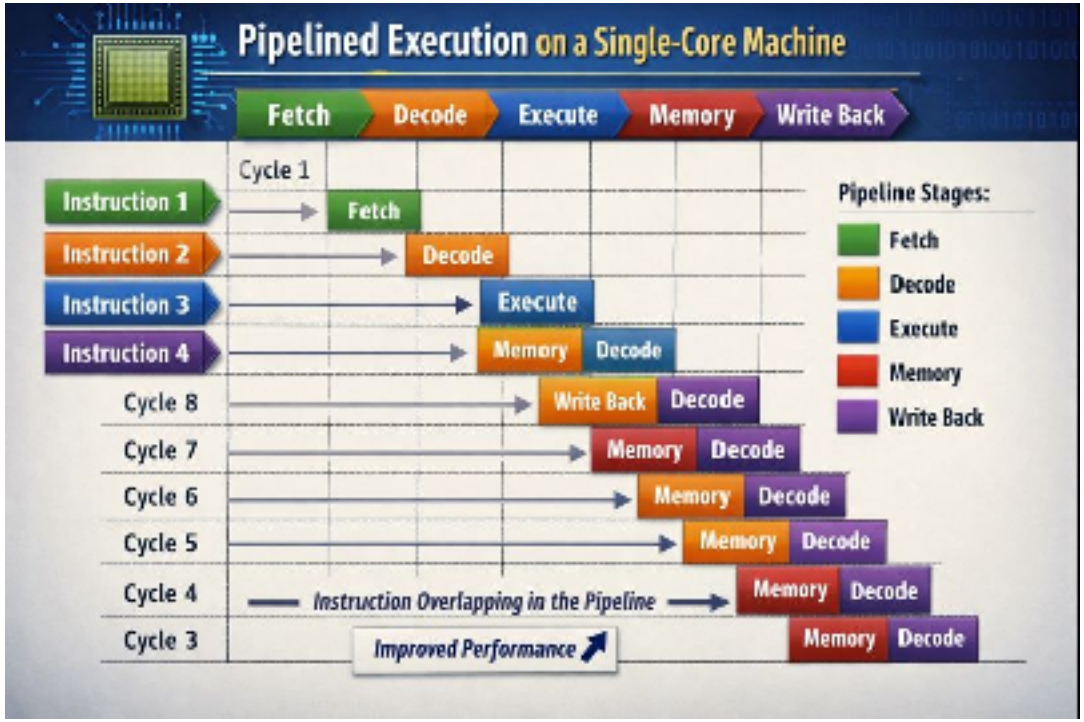
    - What does it mean? We will have to look at how a core is set-up!



Concurrency in Hardware

Superscalar Architectures

- **In single cores** — pipelining of Instruction execution
- Key take-away - **parallelism due to staged execution**
- **Superscalar:**
  - Multiple instruction streams



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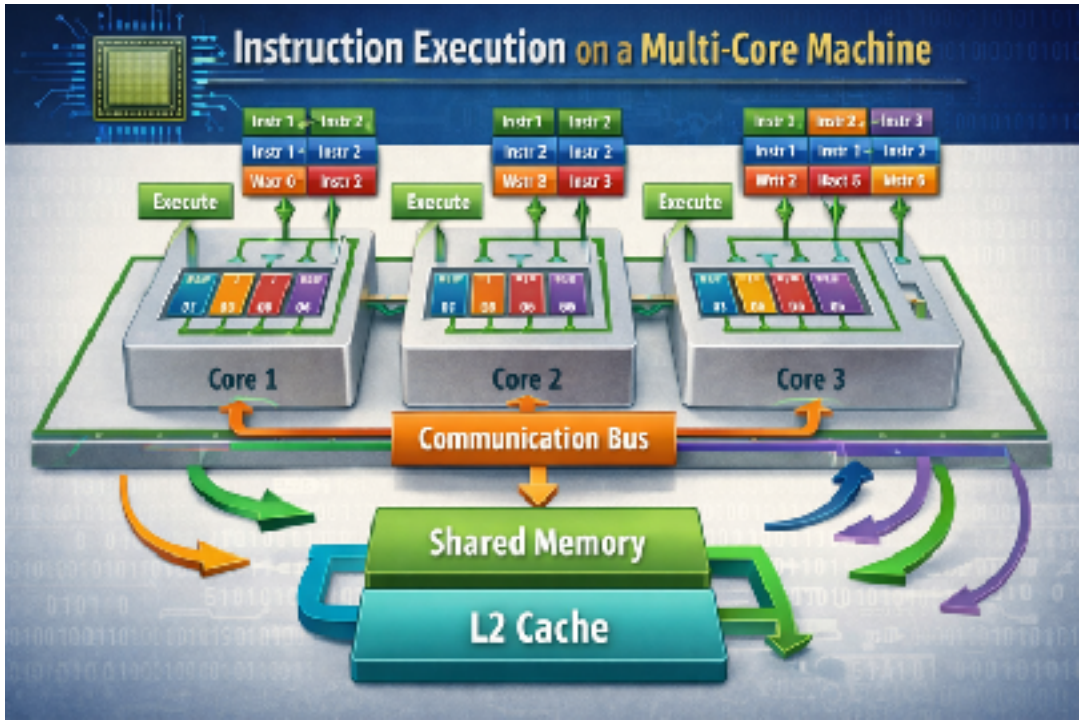
MultiCore Architectures

- **Multiple cores**
- **Each core may be superscalar**
- **Complex:**
  - DMA/Memory Controllers
  - Memory **coherence & consistency**



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void multi_transform(int *input, int *out1, int *out2, int *out3, int n)
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  for (int i = 0; i < n; i++) {
     out1[i] = input[i] * 2; // Double
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- Can execute each loop instruction in parallel — Why?

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  - Could also be **vectorized** on a single-core machine

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